This Page Is Inserted by IFW Operations
and is not a part of the Official Record

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

As rescanning documents *will not* correct images, please do not report the images to the Image Problem Mailbox.

32310_EU_J

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
6 December 2001 (06.12.2001)

PCT

(10) International Publication Number
WO 01/93242 A1

(51) International Patent Classification[7]: G09G 5/00

(21) International Application Number: PCT/US01/17816

(22) International Filing Date: 1 June 2001 (01.06.2001)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
09/587,376 1 June 2000 (01.06.2000) US
09/788,054 16 February 2001 (16.02.2001) US

(71) Applicant *(for all designated States except US)*: **ADVANCED OPTICS ELECTRONICS, INC.** [US/US]; Suite 4, 8301 Washington N.E., Albuquerque, NM 87113 (US).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **HARMON, Michael, G.** [US/US]; 6000 Coraderia, N.E., Albuquerque, NM 87111 (US). **MILLS, Stephen, L.** [US/US]; 212 Richmond, S.E., Albuquerque, NM 87106 (US).

(74) Agent: **MYERS, Jeffrey, D.**; Peacock, Myers & Adams, P.C., P.O. Box 26927, Albuquerque, NM 87125-6927 (US).

(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZW.

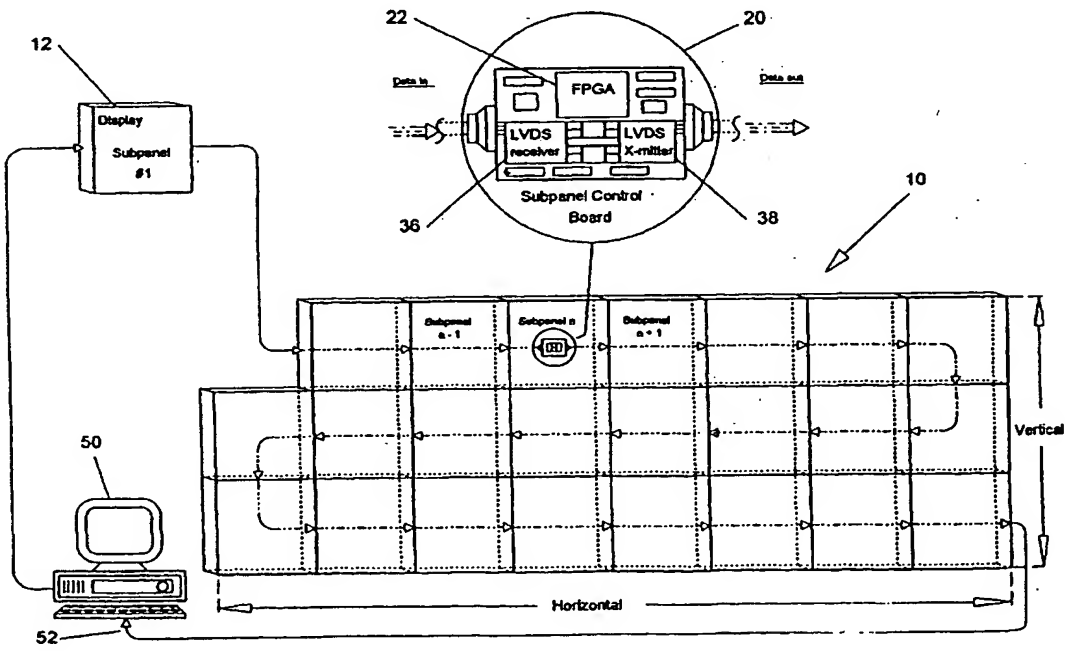
(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

Declaration under Rule 4.17:
— *of inventorship (Rule 4.17(iv)) for US only*

Published:
— *with international search report*

[Continued on next page]

(54) Title: LED CONFIGURATION FOR LARGE-SCALE DISPLAY



(57) Abstract: A method and apparatus for data distribution to a large-scale display (10). Position-independent sub-panels (12) operate in conjunction with a low voltage digital signaling digital video interface. A serial string of transmitter/receiver pairs (36, 38) allow the sub-panels (12) to receive image data from a host computer (50) and relay the data to adjacent sub-panels (12).

WO 01/93242 A1

BNSDOCID: <WO___0193242A1_I_>

before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

LED CONFIGURATION FOR LARGE-SCALE DISPLAY

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a continuation-in-part application of U.S. Patent Application Serial No. 09/587,376, entitled "Data Distribution for Large-Scale Display", to Michael G. Harmon et al., filed on June 1, 2000, and the specification thereof is incorporated herein by reference.

BACKGROUND OF THE INVENTION

Field of the Invention (Technical Field):

The present invention relates to large-scale displays, and particularly for distributing digital display data using a unique method of asserting image intensity data in a bit-by-bit fashion, according to bit position, with microcontrollers and latches to implement pulse width modulation. The invention also includes a unique position-independent sub-panel configuration to manage data position information as well as a global control voltage for further adjustment of the display brightness necessary to adjust to ambient light conditions.

Background Art:

The current state of the art large scale display systems are almost universally light emitting diode (LED) based systems. An LED is a current device and requires a minimum current passing through its diode junction in order to emit any light. It also has a maximum rated current that the manufacturer allows if the LED is to meet stated lifetime and brightness specifications. For applications that require varying intensity emissions, there are two general approaches.

One approach in the prior art is to add circuitry external to the LED that varies the current that passes through the LED from the highest (brightest) to the lowest (dimmest) desired levels. This circuitry can in turn be controlled by a low voltage data signal such as a common video signal. The disadvantage to this method is that, while the current can be varied through the LED it requires many components per LED, a complex analog signal delivered to each LED, and is inherently less efficient

than the pulse width modulation method discussed below due to higher power dissipation in the control circuitry. A large display system might have over a million LEDs and every extra component and milliwatt per LED is significant in the overall cost.

Typically in the prior art, the preferred method for varying the intensity of an LED is with pulse width modulation (PWM). A circuit is designed that gates the maximum desired current (brightness) through a given LED for a period of time, then gates it off for another period of time, the ratio of which is proportional to the desired brightness level for that LED compared to the maximum possible desired intensity value. Thus, if a brightness of a red LED presenting its share of color in the image of an apple has a desired red intensity level of, for example, 80%, the PWM circuit would blink that LED on and off at high speeds with the "on" periods being four times as long as the "off" periods. For example, an LED could be driven at its full intensity for a period of time proportional to its 8-bit subpixel intensity value divided by 256 and left in the off state for the remainder of the given period of time by a typical industry standard PWM integrated circuit (IC) chip as described below. Most displays use PWM ICs which are designed to drive their pixels at relatively high rates, typically 5 kHz, with the appropriate duty cycle determined by a PWM chip for every subpixel.

PWM achieves two savings over a variable current control circuit scheme. First, the power (voltage multiplied by current) under the PWM scheme is dissipated almost entirely in the LED no matter what the desired brightness level, while the variable current scheme, by definition, must dissipate a certain percentage of its power in the current control circuitry proportional to the voltage drop across the circuitry which it must increasingly invoke as it decreases current flow to the LED. Second, the PWM simpler drive scenario allows a significant savings over a variable current circuit due to its compatibility with the more cost-effective digital distribution of the image data and, perhaps more significantly, due to the prior development by the laptop computer industry, of a compact 8-pin, two channel, dual counter/comparator PWM integrated circuit chip, to control the back-lighting in laptop liquid crystal display (LCD) panels.

The typical PWM IC takes in an 8-bit subpixel brightness intensity value into one of two high-speed internal counters and compares its count down to zero to those of the second synchronized

counter which is pre-set to the 8-bit maximum (256) each time it's count reaches zero. The LED is initially turned on for as long as the counter holding its 8-bit brightness value is non-zero and then is turned off when it arrives at zero. It is then left in the "off" state until the maximum value pre-set counter arrives at zero, whereupon both counters are reloaded with their initial values and the process is repeated. This process is continued at very high clock rates until a new subpixel intensity data byte arrives and is loaded into the data value counter.

PWM ICs are almost universally employed in high-resolution, high-speed, large-scale LED displays. A PWM IC is placed at the control input of each LED constant current drive circuit and can be serially loaded with the desired pixel data. Typically, one PWM IC has two separate counter pairs and can control two LEDs. The prior art usage of PWM ICs is shown in Fig. 4a. Red (R), green (G), and blue (B) LEDs are shown generally at **70** and PWM ICs are shown generally at **72**. Once loaded, the IC controls the proper PWM "on/off," or duty cycle, durations for the two LEDs until it is reloaded with the next frame's data values for its two subpixels.

In this above-described manner, the LED controlled by the PWM IC is in the "on" state for a fraction of the entire PWM period, equal to LIV/256 (LED Intensity Value), and is in the "off" state for a fraction of the overall time that is equal to (256-LIV)/256. The illumination intensity ratio or optical "duty cycle" is defined as the "on" state period over the total period as described above as LIV/256. Thus, the LED duty cycle is equal to its intensity value.

This cycle of countdowns is typically repeated at 5,000 countdown (PWM) cycles per second for a count clock rate of over 1 MHz. This rate is used for liquid crystal display (LCD) backlighting because it is better than twice the rate at which the eye can detect moiré jitter, aliasing or image picketing from rapid eye movements. The industry PWM IC is used to meet this need for high frequency PWM cycles.

For a microcontroller running at 4 million instructions per second (MIPS) to perform the same task as the PWM IC, it would need to execute a minimum of 3 instructions (two decrement instructions and zero bit test instruction) to test a given 8-bit subpixel intensity data value and its

associated maximum period value for every one of the 256 possible duty cycle values for an overall requirement of 768 instruction executions per subpixel intensity data value, or 1,536 instructions for two subpixel intensity data values. At an instruction execution rate of 4 million per second it would take the typical microcontroller 0.38 milliseconds to establish a single pulse-width modulated duty cycle for two LEDs, with a resulting sub-standard cycle rate of 2,604 Hz. As such the typical microprocessor cannot be expected to decrement and test all 256 possible states of just two, 8-bit color intensity values, and test each time for zero counts, nearly as efficiently as the 0.2 millisecond cycle period and 5,000 Hz cycle rate demonstrated by PWM ICs.

The dedicated PWM IC method requires a microcontroller and distribution system of intelligent control and data buffering electronics to route and time each data byte to each of the PWM ICs. While the majority of the electronics cost is in the PWM ICs, the microcontroller, distribution and timing electronics are necessary components to any large-scale display system. It would be beneficial to eliminate or replace PWM ICs with a cheaper component for significant savings. The present invention provides an alternative to using the PWM ICs of the prior art as well as a high speed unique configuration for full color, full motion and reproduction of images onto a large scale display.

Patents related to the field of displays and the data distribution and drive electronics include U.S. Patent No. 5,990,802 to Maskeny entitled "Modular LED Messaging Sign Panel and Display System" which discloses a messaging board display using uniquely addressed microcontrollers for each panel, but has no gray scale and limited frame rates. The present invention provides full color, full motion video display. The present invention uses the relative position of the data in the overall data stream to determine if the given data unit is designated for a given sub-panel, while Maskeny simply shifts serial data it receives directly into latches in a serial format. While latches are used to drive the LEDs in the Maskeny display, they are used only to select a given LED for full illumination or not, with minimum illumination periods in the hundreds of milliseconds, and are not pulse width modulated for gray scale presentations in fractions of milliseconds. The latches in the present invention are state registers for the pulse width modulation duration data that, in turn, drive

sophisticated, high-efficiency, amplifier circuits, scaleable for overall brightness adjustment in response to ambient light conditions.

U.S. Patent No. 5,250,939 to Takanashi et al. entitled "Drive Apparatus for Optical Element Array" discloses a pulse width modulation scheme using dual clocks per subpixel to determine duty cycle and therefore subpixel intensity, unlike the bit position processing solution for given subpixel intensity data of the present invention. U.S. Patent No. 5,309,151 to Aoki entitled "Current-Supplying Integrated Circuit" addresses current control for a laser printer diode array which is unlike the unique pulse width modulation scheme of the present invention. U.S. Patent No. 5,327,155 to Olsson et al. entitled "Device for Displaying a Parameter Value" describes a position-addressable illumination scheme to check for inoperable pixels. U.S. Patent No. 5,724,055 to Omae entitled "Display Apparatus and Method of Manufacture in Which Display Luminance Can be Adjusted" describes a preconditioning circuit for normalizing the variations in a given batch of surface-mounted LEDs.

U.S. Patent No. 5,751,263 to Huang et al. entitled "Drive Device and Method for Scanning a Monolithic Integrated LED Array" discloses a scheme by which to select a given pixel element in a row-and-column addressing scheme. The present invention addresses every pixel element individually. The Huang patent cannot deliver a sufficiently strong signal for a long enough period of time to each LED to allow for full color, full motion, daylight operational video display.

U.S. Patent No. 5,808,591 to Mantani entitled "Image Display Device, Image Display System and Program Cartridge Used Therewith" describes a portable game display. U.S. Patent No. 5,889,694 to Shepard entitled "Dual-Addressed Rectifier Storage Device" describes a rectifier storage device having diode junctions used as digital memory latches. U.S. Patent No. 5,812,105 to Van deVen entitled "LED Dot Matrix Drive Method and Apparatus" discloses a power supply-based pulse width modulation scheme supplying voltage to commonly-connected LEDs.

U.S. Patent No. 5,966,110 to Van Zalinge entitled "LED Driver" uses many discrete components per LED with an analog driver scheme and is costly compared to the digital configuration of the present invention. U.S. Patent No. 5,836,676 to Ando et al. entitled "Light Emitting Display

Apparatus" uses two LEDs per pixel, rather than three and is not a true color display. This patent relates to the use of LEDs to produce image displays. U.S. Patent Nos. 5,724,062 and 5,359,345 both to Hunter entitled "High Resolution, High Brightness Light Emitting Diode Display and Method and Producing the Same" and "Shuttered and Cycled Light Emitting Diode Display and Method of Producing the Same" respectively, disclose LEDs employed as a back light for a liquid crystal shutter-type display.

U.S. Patent No. 5,722,767 to Lin entitled "LED Display Panel Structure" describes an LED mounting scheme for ensuring a weather-tight display which requires that the subpixels be spaced at a significant distance from one another and therefore provides a relatively low brightness large pixel display. U.S. Patent No. 5,717,417 to Takahashi entitled "Dot-Matrix LED Display Device Having Brightness Correction Circuit and Method for Correcting Brightness Using the Correction Circuit" discloses a pulse-width modulation approach wherein LEDs are sequentially scanned. Takahashi emphasizes correcting intensity differences among individual LEDs and stores correction data in read-only memory. U.S. Patent No. 5,708,452 also to Takahashi entitled "LED Display Device and Method for Controlling the Same" uses analog switches to send analog signals to the display and does not employ digital methodology.

U.S. Patent Nos. 5,278,542 and 5,134,387 both to Smith et al. entitled "Multicolor Display System", both disclose a pulse-width modulation method based on a frame-by-frame mode rather than by a pixel-by-pixel mode as in the present invention. The two patents disclose a fundamentally low duty cycle method and will result in relatively low brightness. These patents also only employ two LEDs per color pixel.

U.S. Patent No. 5,008,595 to Kazar entitled "Ornamental Light Display Apparatus" discloses the use of a common power bus modulation scheme for different color LEDs. It is pulse width modulation synchronized with supply side multiplexing. U.S. Patent No. 5,184,114 to Brown entitled "Solid State Color Display System and Light Emitting Diode Pixels Therefor" discloses a "phase-modulated light" LED matrix and pulse width modulation using shift registers and latches and storing and reading the image out of random access memory. The '114 patent employs a row/column matrix

approach for driving the LED elements, unlike the present invention which drives each LED element individually.

U.S. Patent No. 4,982,182 to Flinois entitled "Directly Driven Light Emitting Diode Array" discloses an inexpensive scheme wherein D-type latch outputs are used as an unregulated current source for the LEDs. U.S. Patent No. 4,924,217 to Uwai entitled "Driver Circuits for Dot Matrix Display Apparatus" discloses a row-column addressing scheme used with an exotic carry-bit scheme. The present invention uses a separate driver for each subpixel. U.S. Patent No. 4,887,074 to Simon et al. entitled "Light-Emitting Diode Display System" uses an alternating current drive scheme rather than a direct current drive method as in the present invention. U.S. Patent No. 4,506,955 to Kmetz entitled "Interconnection and Addressing Scheme for LCDS" discloses a row/column matrix approach for illuminating liquid crystal diode cells, which, again, is unlike the present invention which individually actuates each LED element. U.S. Patent No. 4,394,600 to Flannagan entitled "Light Emitting Diode Matrix" discloses a mechanical physical mounting method for LED arrays using common anodes on an aluminum substrate.

The present invention overcomes the limitations of prior art pulse width modulation and of the patents discussed above. The present invention performs the pulse width modulation process, but replaces PWM ICs with standard 74 series octal latches that service eight LEDs per IC for a significant cost savings per pixel. These standard octal latches are relatively inexpensive.

The present invention is further a unique method of extracting the PWM duty cycle from the 8-bit intensity data in a bitwise fashion rather than in the traditional incremental fashion. Instead of decrementing each color intensity byte through all 256 possible states to establish the PWM duty cycle, the data byte is processed in a bit-by-bit manner for only eight total states of interest which provides all the necessary duty cycle information for a geometric increase, which is 32-fold for 8-bit data, in PWM generation efficiency. In this fashion a high-performance microcontroller and 24 octal latches can replace 96 PWM ICs for images control of 64 pixels and provide a significant cost savings. Pulse width modulation using the countdown method, which is virtually the only method currently employed in either hardware or software PWM implementation schemes, would take a

microcontroller at least 500 times as many instructions to implement over the method of the present invention. Practically speaking, this allows for an order of magnitude increase in the large scale display resolution at no additional cost with respect to drive electronics. Currently, most large scale video displays use one PWM IC to control large clusters of LEDs, up to 10 per color, or 30 per pixel, with the spacing between each pixel being one to two inches, for a resulting density of, at best, one pixel per square inch. For the same overall cost the display of the present invention will drive one LED per color with a pixel spacing of approximately 3.12 pixels per inch, yielding a density of ten pixels per square inch. Therefore, the grainy images of traditional large-scale displays are supplanted by seamless, grain-free resolutions of near-photographic quality when viewed at optimum viewing distances.

SUMMARY OF THE INVENTION (DISCLOSURE OF THE INVENTION)

The present invention is a display and comprises at least one position-independent sub-panel, a digital video interface that distributes digital image data to and from the sub-panel(s), and a host computer that generates and stores images. The host computer also remotely communicates with other systems. The host computer has a controller which delivers the image information to the sub-panel(s). Preferably, a plurality of sub-panels are connected in serial to comprise the display. Low voltage digital signaling is used in the digital video interface, and comprises transmitter/receiver pairs for data distribution across the sub-panel(s). The transmitter/receiver pairs are serial relay pairs. Information is received at each sub-panel and then also transmitted on to the next sub-panel accordingly. The transmitter/receiver pairs are broken down into odd pixel and even pixel transmitter/receiver pairs for optimization of data distribution.

The sub-panels that make up the display, as well as the data distribution methodology of the present invention, comprise a display having a resolution equivalent to that internal to the computer. The display is preferably at least approximately 54 feet by 54 feet in the horizontal and vertical directions. Preferably, the display has a resolution of up to approximately 2,048 by 2,048 pixels. Programmable gate arrays are used to acquire image data appropriate to each of the sub-panels from the overall image data stream. The programmable gate arrays are approximately

instantaneously reprogrammable. FIFO data buffers receive the image data from the programmable gate arrays for the sub-panels.

Each of the sub-panels comprises a plurality of pixels, and further a microcontroller controls image data to a plurality of pixels within that plurality of pixels comprising each sub-panel. The display further comprises a plurality of pixel display elements and a plurality of display element drive circuits for implementing the pulse width modulated image data to the display elements. Each of the display element drive circuits comprises a plurality of latches and associated circuitry for control of each display element.

The microcontrollers implement pulse width modulation of the image data to the pixel display elements by asserting the image data according to bit position. Each of the microcontrollers asserts the most significant bit of a given data byte of image data separately from lesser significant bits. Each of the microcontrollers further asserts image data according to whether the image data is for odd or even pixels on the display.

The plurality of pixel display elements preferably comprise a pixel density of greater than approximately ten pixels per square inch. The display further comprises a global control for adjusting the display brightness according to ambient light conditions.

The present invention is also a method of distributing data to a display and comprises the steps of providing a display comprising at least one position-independent sub-panel; providing a computer for distributing image data to the display; generating images in the computer for distribution to the display;
distributing digital image data between the computer and the sub-panel(s) with a digital video interface; and displaying the images on the display. The step of providing a display preferably comprises providing a plurality of position-independent sub-panels and connecting the sub-panels in serial.

Distributing digital image data comprises distributing digital image data via low voltage digital signaling. The step of low voltage signaling comprises transmitting and receiving with at least one low voltage digital signaling transmitter/receiver pair. Transmitting and receiving comprises transmitting and receiving with serial relay pairs of transmitter/receivers. Transmitting and receiving preferably comprises transmitting and receiving according to odd and even pixels.

The step of displaying the images on the display comprises displaying the images with a resolution equivalent to that internal to the computer. Displaying the images on the display comprises displaying the images on a display that is at least approximately 54 feet by 54 feet in the horizontal and vertical directions, and preferably comprises displaying the images on a display having a resolution of up to approximately 2,048 by 2,048 pixels. However, smaller sizes may be utilized in accordance with the present invention.

The method further comprises acquiring image data appropriate to each of the sub-panel(s) from the overall image data stream. Acquiring image data appropriate to each of the sub-panel(s) comprises acquiring image data appropriate to each of the sub-panel(s) with at least one programmable gate array that is approximately instantaneously reprogrammable.

The method further comprises the step of controlling a plurality of pixels within each of the sub-panel(s) with a microcontroller. The method also further comprises asserting the image data according to bit position. The step of asserting the image data according to bit position comprises asserting the most significant bit of a given data byte of image data separately from lesser significant bits. Asserting the image data according to bit position further comprises asserting image data according to whether the image data is for odd or even pixels on the display. Preferably, the step of displaying the images comprises displaying the images with a pixel density of greater than approximately ten pixels per square inch. The method further comprises adjusting the display brightness according to ambient light conditions.

The present invention is further of a method of distributing data to a display and comprises the step of asserting image data according to bit position. Asserting image data according to bit position

comprises asserting the most significant bit of a given data byte separately from lesser significant bits. This method further comprises the step of asserting image data according to whether the image data is for odd or even pixels on the display. The step of asserting image data according to bit position preferably comprises asserting according to odd and even pixel data and alternating between most significant bits and lesser significant bits in order to increase image data display speed.

The present invention is still further of a color display apparatus and method comprising: providing to a display a plurality of pixels; and providing each pixel with a plurality of subpixels, each subpixel being selected from a group consisting of two or more colors, wherein a color arrangement of the subpixels is not homogenous across all pixels. In the preferred embodiment, each pixel has four subpixels, two red, one green, and one blue, and odd numbered pixels in a row or column differ from even numbered pixels in the row or column in that blue and green subpixels are reversed. The non-homogeneity prevents color distortion of the display if the row or column is occluded or partially occluded to a viewer.

The invention is additionally of a color display apparatus and method comprising: providing to a display a printed circuit board; and mounting a plurality of LEDs to an edge of the printed circuit board and orienting the LEDs parallel to the printed circuit board. In the preferred embodiment, a plurality of LEDs is mounted to both sides of the edge of the printed circuit board, the two adjacent LEDs on one side of the printed circuit board and two adjacent LEDs on the other side of the printed circuit board together make up a pixel of the display. Leads of each LED are left unbent and are affixed to conductive pads of the printed circuit board such that the unbent leads do not extend past the interior ends of the conductive pads. The unbent leads and the conductive pads dissipate heat produced by the LEDs during operation of the display. The resulting display has a brightness of at least approximately 5,000 lumens/m^2, preferably between approximately 5,000 lumens/m^2 and approximately 50,000 lumens/m^2. The very same printed circuit board preferably includes the drive electronics, which permits minimization of the total path length of the conductive paths between the LEDs and the drive electronics.

The invention is further of a display apparatus and method comprising: providing to a display first and second printed circuit boards; and providing to the first and second printed circuit boards a plurality of LEDs each comprising leads connected to and passing through the first printed circuit board and affixed to the second circuit board; and thereby creating a plenum in the space between the first and the second printed circuit boards.

The invention is additionally of an LED display apparatus comprising a brightness of at least approximately 5,000 lumens/m^2. In the preferred embodiment, the brightness is between approximately 5,000 lumens/m^2 and approximately 50,000 lumens/m^2.

A primary object of the present invention is to control a greater number of pixels than the prior art using less expensive drive electronics.

Another object of the present invention is to increase resolution, brightness, and overall size of the display with little or no increase in cost of the drive electronics.

An additional object of the present invention is to provide higher frame rates than available in the prior art.

A further object of the present invention is to provide LED displays that dissipate heat efficiently.

Yet another object of the present invention is to provide displays that do not have color distortion when parts of the display are obscured to a viewer.

A primary advantage of the present invention is increased display resolution having little or no additional cost allocated to drive electronics.

Another advantage of the present invention is to increase the overall size of the display at little or no additional cost over prior art systems.

Still another advantage of the present invention is that it delivers higher frame rates than in the prior art.

Other objects, advantages and novel features, and further scope of applicability of the present invention will be set forth in part in the detailed description to follow, taken in conjunction with the accompanying drawings, and in part will become apparent to those skilled in the art upon examination of the following, or may be learned by practice of the invention. The objects and advantages of the invention may be realized and attained by means of the instrumentalities and combinations particularly pointed out in the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are incorporated into and form a part of the specification, illustrate several embodiments of the present invention and, together with the description, serve to explain the principles of the invention. The drawings are only for the purpose of illustrating a preferred embodiment of the invention and are not to be construed as limiting the invention. In the drawings:

Fig. 1 is a diagram of the preferred embodiment of the present invention showing uniform sub-panels and digital video interface data stream flow;

Fig. 2 is a block diagram of the electronics of the preferred embodiment of the present invention showing control by a host computer, sub-panel control and horizontal line pixel control;

Fig. 3 is a software flow chart showing the pulse width modulation scheme of the present invention;

Fig. 4a shows the prior art method of controlling LEDs with pulse width modulation integrated circuits;

Fig. 4b is a diagram of the preferred embodiment of the present invention showing LEDs driven by latch integrated circuits;

Fig. 5 is a schematic of the subpixel drive circuitry regulating the current to each LED in accordance with the preferred embodiment of the present invention;

Fig. 6 is a perspective view of the alternate subpixel color arrangement of the invention;

Fig. 7 is a top view of the edge-mounted LEDs of the present invention;

Fig. 8 is a front view of the edge-mounted LEDs;

Fig. 9 is a bottom view of the edge-mounted LEDs;

Fig. 10 is a side view of the edge-mounted LEDs; and

Fig. 11 is a cut-away perspective view of the lead-vaned heat convection plenum of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS (BEST MODES FOR CARRYING OUT THE INVENTION)

Display

Attention is now turned to Fig. 1 which shows the present invention formatted for a typical billboard macro-display **10**. Universal position-independent sub-panels represented by *n*, *n* + 1, etc. make up display **10**. Host PC **50** contains a controller, such as a digital LCD panel controller, and communicates with display sub-panel control accomplished with an industry standard digital video interface (DVI). DVI is a specific instance of LVDS (low voltage digital signaling, also known as transition minimized digital signaling (TMDS)) and as will be readily understood by one of ordinary skill in the art, LVDS implementations other than DVI may be employed with the present invention. The controller and preferred DVI data distribution ICs are discussed further below. PC **50** is provided

with a modem or Internet link for hack-proof remote programming of the screen content, system diagnostics, software and firmware upgrades, and access to unit history from any laptop or desktop computer. Full-frame digital image data is relayed throughout display **10** by DVI transmitter/receiver pairs. The upper left display sub-panel **12** is linked to the host PC **50** by the host PC's DVI transmitter. DVI receiver/transmitter pairs are provided for each sub-panel. Upon initial power up, phase relative position data is intercepted and passed to the next sub-panel "downstream" for sequential, auto-configuration by each sub-panel for exact determination of the spatial context for the sub-panel within the overall image. This allows for appropriate pixel selection from the data stream.

In the horizontal direction, there are shown eight sub-panels. This number of sub-panels is expandable to sixteen. It would be apparent to those skilled in the art that the present invention can accommodate any number of sub-panels in the horizontal and vertical directions. If each sub-panel has 128 x 128 pixel resolution, then eight sub-panels provides a total horizontal resolution of 1,024 pixels. Fig. 1 shows three sub-panel rows in the vertical direction for a vertical resolution of 384 pixels. This too can be expanded to sixteen panels in the vertical direction for a maximum vertical resolution of 2,048 pixels. The aspect ratio and size shown in Fig. 1 dictates an area that is only 1/10 the maximum capability of the present invention. Current industry standard flat panel controllers allow display resolutions up to 2,048 x 2,048, or 16 x 16 sub-panels at 41 inches x 41 inches each, for a display size of 54 feet x 54 feet. Of course, the size of the display can be based on any combination of subpanels of any size.

While preferred and exemplary numbers of data bits and bytes, subpixels and pixels, pixels per row and half-row, numbers of rows and half-rows, and quantities of sub-panels are used herein, the invention is not to be limited to these quantities.

The signal distribution scheme of the present invention preferably uses the DVI standard, differential signaling, digital data distribution scheme. The standard DVI implementation has a transmitter IC at the source of the video data stream and a receiver at the destination. Each of the display sub-panels have a receiver **36** and a transmitter **38** on each sub-panel control board that

receives its data from either host PC **50** or an adjacent sub-panel, which it will in turn relay via its transmitter to the next sub-panel in line or back to PC **50**.

Sub-panel *n* is expanded in Fig. 1 to show a portion of sub-panel control board **20** having field programmable gate array (FPGA) **22**, DVI receiver **36**, and DVI transmitter **38** to be discussed in further detail below. Programmable control devices other than FPGAs may be employed, e.g., microprocessors. Data is received into sub-panel control board **20** and displayed and distributed as follows. Position information from sub-panel *n* - 1 is inserted into the data stream on the otherwise idle DVI special feature control lines and is intercepted by sub-panel *n* to determine the proper position in the image stream of pixel databytes that must, by definition, pass transparently through the DVI relay ICs. This is analogous to days of a calendar year passing by a square on the calendar until its day arrives and it is marked off. In this manner, sub-panel *n* + 1 will have received at power-up, unique position information yet receive that information in the identical process that sub-panel *n* (or *n* + *x*) received its positional information. Thus, all sub-panels are constructed identically and assembled in any order or position on display **10**, making them universal and position-independent. The position of each sub-panel is therefore established solely by the simple geometry of the DVI cable routing and universally responsive hardware algorithms programmed into the FPGAs on each sub-panel control board, from one sub-panel row to the next as shown in Fig. 1.

As shown by link **52**, the DVI stream returns to PC **50** delivering diagnostic data from each sub-panel on the same spare DVI lines, as will be discussed in further detail below. Again, each sub-panel can be approximately 1 square meter and each is driven independently. Sub-panels can of course be any dimension, such as from approximately ¼ square meter up to 4 square meters. Display **10** can comprise any number of sub-panels from 1 to 400 or more.

Controller

A large scale display system presents challenges with respect to data distribution and drive electronics. Several front-end video data formats are available such as NTSC, which is a television video format, RGB which is a cathode ray tube computer display format, and the digital flat panel computer display format. For displays used primarily for advertising, the inexpensive on-site

personal computer (PC) **50** is most advantageous for image generation, storage, and remote communications by modem with the display **10**. For this and several other reasons the digital format of the standard, commercially available LCD panel controller as part of the PC is used in the present invention to deliver the image information to display **10** to provide full motion video. The present invention accommodates currently available controllers having frame rates up to 85 Hertz, but is adaptable to accommodate even higher frame rates as they become available.

The standard PC-based, digital flat panel controller utilizes two separate data busses, one for odd pixels and the other for even pixels. Each bus consists of three timing signals (frame sync, line sync, and data clock) and 24 color intensity bits (eight red, eight green, and eight blue) to deliver image data to the typical flat panel, LCD or plasma, display. Employing the DVI (or other LVDS based standard) image data distribution standard allows the LED drive circuitry of the present invention to use the same data identically as that generated by the LCD panel controller for unmodified, faithful full color reproduction of the imagery internal to PC **50**, up to 1,600 x 1,200 resolution, with sixteen million color shades, dependent only upon the quality of the controller. The ability to produce an image on a display having a resolution equivalent to that internal to the computer is a significant advancement over simple messaging boards. Another advantage in using the digital flat-panel controller format for driving the large-scale display system is in data distribution.

In the prior art, the increased bandwidth required for high resolution LCD panels, up to 3 million color bytes per frame, made it necessary for the panel to be nearby, preferably within inches, of the central processing unit (CPU) motherboard for undistorted TTL signaling. In order to facilitate a variety of flat panel applications, the industry currently employs a data transmission scheme using low voltage, differential signaling over a twisted pair medium. With the sheer physical size of the large-scale display there arises a non-trivial problem of conveying very high speed data over considerable distances without appreciable signal degradation. For this reason, DVI is accomplished by using low voltage digital signaling (LVDS) transmitter/receiver pairs in the preferred embodiment of the invention. While these are intended for freeing display **10** from remaining tightly tethered to the CPU, they are further used in serial relay pairs in the present invention for data distribution across multiple panels of a vastly larger display area.

Pixels and Sub-panels

The present invention also uses a smaller diameter pixel size than in the prior art. Attention is now turned briefly to Fig. 4b where pixels are shown generally at **70** by red, green, and blue LEDs. The pixel size is preferably approximately 0.32 inches in diameter and each pixel preferably consists of green, blue and red LEDs. While LEDs are discussed throughout, other pixel display elements can be substituted in accordance with the invention, such as surface mount LEDs, plasma discharge cells, and miniature fluorescent bulbs. Preferably the green and blue LEDs are extra bright. The invention can accommodate smaller diameter pixel sizes as smaller and brighter LEDs are developed. Furthermore, as brighter red LEDs become available, the invention can accommodate fewer red LEDs per pixel.

In the preferred embodiment, pixel spacing is approximately 3.12 pixels per inch yielding a density of approximately ten pixels per square inch. The preferred embodiment of the present invention uses one "bright" green, one "bright" blue, and two "bright" red LEDs per pixel. Two red LEDs provide an equivalent brightness to the single green or blue LED. This configuration is chosen because these LEDs are currently available in the industry. While Fig. 4b shows only one red (R) LED per latch integrated circuit (IC), latch IC shown generally at **74** can drive two in place of each one. Other LED color configurations would be apparent to those skilled in the art. The invention is not to be limited to three basic subpixels, nor by the number of LEDs driven by the latch ICs.

LEDs are current-driven devices and require a separate driver for each individual diode. Thus, individual pixel data must be distributed, stored and translated into durational dwell times, or light intensities, for each LED causing a bottleneck to form at the pixel level. This multiplicity of elements and related tasking densities, coupled with the relatively large distances between pixels on each end of a long row hampering high-speed printed circuit design and exacerbating inherent noise issues, limits the number of pixels that may be serviced in a given period of time or physical space by a dedicated logical resource, such as a microcontroller, state machine, or specialized device. This limitation, coupled with manufacturing considerations for sub-assemblies of practical dimensions, made splitting display **10** into the sub-panels most practical.

As an example, 72 separate data paths are required, one between each sub-panel, of a display having 72 sub-panels. As discussed above, the LVDS transmitter/receiver pairs are preferred for a lossless digital data distribution scheme to the sub-panels. A series of transmitter/receiver pairs is employed on sub-panel control board **20** near PC **50** to distribute the data stream through each sub-panel.

In order to allow independent frame timing for each sub-panel, the appropriate pixel data bytes that correspond to the row and column positions occupied by a given sub-panel within display **10** must be sifted from the incoming data stream and buffered for immediate sub-panel use. Due to the speed at which the incoming data needs to be processed, a state machine (a highly specific digital circuit) approach is used for timing and overall data flow instead of microprocessor control. A large, high-speed FPGA is used to accomplish this task.

Attention is now turned to Fig. 2. Fig. 2 shows the internal electronics of an individual position-independent sub-panel. Each sub-panel's data distribution electronics are contained on a single sub-panel control board. All sub-panel data selection/control boards are physically identical. PC **50** having the internal LCD panel controller transmits the digital data stream to the DVI transmitter that is within PC **50** to the first sub-panel **12** shown in Fig. 1. Sub-panel control board **20** is shown with high-speed first-in first-out data buffers **24** and **26**, FPGA **22**, DVI receiver **36** and DVI transmitter **38**. Sub-panel control board **20** controls 256 partial rowboards, which in this embodiment are horizontal half-line pixel control rowboards **40**, each of which contain a microcontroller, shift register, latches and actual LED pixels and are shown generally at **42**. Two half-line rowboards comprise one sub-panel horizontal line. Each sub-panel contains a data distribution control board and 256 horizontal half-line rowboards for a total of 128 horizontal lines. The computer based DVI sub-panel transmitter shown in Fig. 2 is the first in a serial string of transmitter/receiver pairs, one for each sub-panel, which receive the image data from the preceding sub-panel, or PC **50** if it happens to be the upper left sub-panel, while simultaneously transmitting the data onto the next sub-panel, or back to PC **50** if it happens to be the bottom right sub-panel.

As the two, odd and even pixel, incoming data streams arrive at a given sub-panel's DVI receiver, shown at **28** and **30**, they are immediately applied to the input register pins of two, 8 kilobyte, high-speed first in first out (FIFO) data buffers **24** and **26**. Odd and even pixel DVI transmitters are shown at **32** and **34** respectively. The depiction of separate components for odd and even pixels will be further described below. Inappropriate data that is not associated with a given sub-panel's physical location within display **10** are ignored and desired data are strobed into FIFOs **24** and **26** by FPGA **22**.

In the example display configuration with 72 sub-panels, there are up to 72 different programming configurations for each FPGA **22** depending upon its respective sub-panel's location within display **10**. After the first odd and even pixel data pair are selected and entered into the buffers from the incoming data stream, a sub-panel frame start bit is set by FPGA **22** and pixel data is clocked into the half-row microcontrollers at up to 1/72nd the incoming pixel rate. The data stream is relayed to the adjoining sub-panel as shown at **46**.

FPGA **22** contains the position sensitive circuitry for appropriate acquisition of pixel data intended for illumination within the confines of a particular sub-panel from the overall data stream. FPGA **22** receives its position data from unused channels on the LVDS data stream for automatic, independent determination of initial position data, or subsequent special purpose revisions, for example such as picture-in-picture or resolution changes.

The FPGAs can be reprogrammed rapidly, in as short a time as less than twenty seconds, as needed for screen partitioning and multiple sourcing. JTAG files, the data format for programmable logic arrays, for reprogramming the FPGA **22** on each sub-panel are held in the hard disk of PC **50** and each sub-panel control board is provided with a modest watchdog microcontroller for reprogramming and diagnostics. In this manner each sub-panel can be reassigned for resolution and frame position to act as a smaller picture within a picture or as a split screen, or to take a separate video stream from the other sub-panels.

In the preferred embodiment, each sub-panel comprises 256 horizontal half-line pixel rowboards, each being 64 pixels long, but the invention is not to be limited to this number of rowboards or to this number of pixels per rowboard or half-line rowboard. The two horizontal half-line pixel rowboards, "a" and "b," make up a full horizontal line of 128 pixels. Each of the two rowboards has its own microcontroller (driving its 64 pixels). Once the data for one rowboard is loaded into the appropriate microcontroller, a bit is shifted into the next rowboard to initiate its data flow cycle, as the previous row begins the illumination process for its LEDs. Grayscale illumination is achieved by running the LED at full illumination for a portion of the overall frame interval equivalent to the subpixel intensity value divided by 256, for an 8-bit per color format producing an overall color resolution of 16 million colors. This process is repeated 256 times for each subsequent sub-panel rowboard until a full sub-frame of data has been illuminated. While 8-bit data bytes are discussed herein, it is to be understood that any number of bits per byte can be accommodated with the present invention.

Attention is now turned to Fig. 3. Fig. 3 is a software flow chart for the unique pulse width modulation scheme of the present invention wherein subpixel data is examined in a bit by bit fashion. The software is in microcontroller assembly language and can be implemented with, for example, a Microchip™ PIC microcontroller. In the "Get Data" block, a signal interrupts the microcontroller, and 192 bytes of data, that is 64 pixels with three colors per pixel, are read from an input/output port and stored in RAM. The interrupt occurs at the frame rate dictated by the flat panel controller in the host PC. In the pulse width modulation output block after "Get Data," a signal occurs at approximately 16 kHz that synchronizes the PWM output fields (odd then even MSB through LSB) into groups, or supersets, of output duration fields that can be executed harmoniously in one 16 kHz cycle period for an overall PWM cycle rate of 4 kHz.

In the present invention, a single microcontroller is used to assert durational dwell times for an entire horizontal half-line of subpixels, which in the present example is 3 x 64 = 192. Normally this would require that each 8-bit subpixel data value be decremented and tested for equality to zero at least 256 times per frame to assure all possible 8-bit subpixel intensity values are fully processed. This approach is prohibitively slow and would result in a worst case pulse rate just over the overall frame rate of 60 Hz.

The present invention overcomes this problem by asserting/de-asserting the subpixel data according to bit position, deriving duration, or dwell time, information in a much faster manner. As used throughout the specification and claims, the term "assert," and forms thereof, is used to indicate either assertion or de-assertion of the bit value at the corresponding pixel display elements. That is, if a given subpixel intensity value is for example 131, and assuming 8-bit data bytes, then there is a "1" in bit 7, a "1" in bit 1, and a "1" in the bit 0 position. Examining this value a bit at a time provides the following information. First, a "1" is encountered in the bit 7 position. Therefore the subpixel will necessarily be in the "on" state, i.e. asserted, for at least one-half the time because the most significant bit in any binary number represents one-half of the overall value. Subsequently, the next "1" in the bit 1 position indicates an additional duration of 1/128 of the time and the last "1" in the bit 0 position indicates a further duration of 1/256 of the time. After asserting all the most significant bits of all the subpixels, nothing needs be performed on those pixels for one-half of whatever cycle time is determined to be the fastest time all the data for a given row can be fully tested and asserted. By approaching half of the pixels from the most significant end and half from the least significant end, a distribution of task can be achieved that allows an effective pulse frequency of 64 times the frame rate using one relatively inexpensive microcontroller per 192 subpixels. This methodology of asserting most significant bits separately from the lesser significant bits allows for the use of a series of 8-bit latches, or 1/8 of a latch IC, to drive each subpixel, for a greatly reduced per-pixel cost in implementing a PWM scheme. This method is of course applicable to digital data bytes of any number of bits, and to pixels having any number of subpixels, and latches of any number of bits, including 16-bit latches, may be employed. The invention is not to be limited to the example subpixel, pixel, half-row, row, sub-panel, latch, and display sizes used herein.

The data is distributed by asserting the most significant bits separately from the lesser significant bits as follows. A data byte is examined for the value of its most significant bit. The value, whether 1 or 0, is sent directly to an octal latch and allowed to assert, if the bit is 1, or de-assert, if the bit is 0, the associated LED drive circuit shown in Fig. 5 which is then allowed to remain in this given state for one-half of the predetermined PWM cycle period, or 0.1 millisecond for a 5 kHz PWM rate. Fig. 5 is described further below. This is relevant because the most significant bit in any multi-bit

binary number represents one-half of its maximum possible value. Subsequently the next most significant bit is sent to the latches and allowed to assert, or de-assert, the LED drive circuitry for one-quarter of a predetermined time period, and so on, until the least significant bit is latched and asserted for, in the case of an 8 bit color intensity data byte, for 1/256th of the predetermined PWM cycle period at which point the duty cycle period will have expired and the process is repeated. In this manner, a given group of eight data bytes is shifted, each in turn, to produce a series of eight adjacent bits all of which are from the same bit position in their respective bytes of origin, which combine to form a latch "byte" of contiguous subpixel bitwise PWM assert bits which are sent to their corresponding LED's latches while a global timer monitors their particular bit position's appropriate assertion period. While the PWM period for those bits is pending, the next eight data bytes are processed for the bits from their currently relevant bit positions. The process is repeated until all the bits from all eight positions have been asserted at their respective LED latches for the appropriate PWM durations. In the preferred embodiment, the optimum duty cycle is approximately 0.26 milliseconds for a 3.8 kHz PWM rate. This duty cycle is preferred because it provides the best balance of cost versus performance, and the invention is not to be limited to this frequency.

Subpixel Drive Circuitry

Attention is now turned to Fig. 5. Fig. 5 is a schematic of the subpixel drive circuitry of the present invention. Each latch gates a current source which regulates the current to its corresponding LED. The current source consists of NPN transistor **82** with a current sensing resistor **84** connected between the emitter and ground, and a reference voltage applied to the base of PNP transistor **88**. LED **80** is connected to the collector of NPN transistor **82**, and therefore the transistor current which is developed will flow through LED **80**. The current in transistor **82** is determined by the voltage generated across current sensing resistor **84**, and this voltage is set by the reference voltage minus the base-emitter diode voltage of transistor **82**. Because the base-emitter diode voltage of a transistor is temperature sensitive, a second, PNP transistor **88** is employed as an emitter follower. The reference voltage is translated upward in value through PNP transistor **88** in the diode junction, and is then translated downward in value through NPN transistor **82**. Although the magnitude of these translations can vary together due to temperature sensitivity of the diode junctions, the translation upward in PNP transistor **88** and the translation downward in NPN transistor **82** tends to

cancel. Therefore, the temperature sensitivity at the output of the current source is largely cancelled. Resistor **86** is typically ten kiloohms, although other values are possible, or other resistors can be used in combination with resistor **86** to accomplish the same result. Other configurations of the subpixel drive circuitry are also possible and the invention is not to be limited to this exact configuration.

The reference voltage inputs of the current sources for a given color are wired together on each rowboard of the horizontal line pixel control board. Output current can thus be turned up or down for all red, green, or blue LEDs in a group by adjusting the reference voltage.

On each row board of horizontal line pixel control board **40** of Fig. 2, the reference voltages are set relative to the grounding point of that circuit board. By this means, the reference voltages are largely immune to fluctuations in the ground potential in other parts of the system, as well as to modest fluctuations in power supply voltages. This is accomplished by an operational amplifier for each reference voltage, configured as a differencing amplifier, with one input set to a control voltage which is global to the display and the other input set to the ground reference at the global control voltage source.

The global control voltage is used to turn the overall display down when ambient light conditions are low, as indicated by a photocell sensing circuit. The display can also be turned down when all or almost all of the pixels are set to maximum brightness and thus maximum current. This allows for lower power requirements than prior art designs based on peak requirements which rarely occur. The power limiting state is activated when the "forced current sharing" control line from the power supply bank indicates a condition of near maximum current output. This control line is commonly found on higher quality commercially available power supplies. While the primary and rapid means of setting the display brightness is by pulse width modulation, the global control voltage affords a secondary, relatively slow method of adjustment that would be difficult to attain using PWM alone.

PWM Optimization - - Odd and Even Pixel Task Groups

Attention is returned to Figs. 2 and 3. A further refinement in the method of the present invention addresses task distribution for optimization of microcontroller overhead. The least significant bits are the most difficult to apply to the latches due to their very brief durations. It is the disposition at the latches of the least significant bits, by virtue of having the smallest (and briefest) contribution to the overall duty cycle that exerts the greatest demand for speed from the microcontroller.

One way to increase the apparent processing speed is to distribute the peak processing periods into odd and even pixel task groups for a 50% reduction in the processing time for all tasks, but most importantly, the most speed-intensive tasks. Thus, the microcontroller first asserts only the MSB (bit 7) of the odd pixels at their respective latches, thereby controlling the corresponding pixel display elements accordingly, then ignores them for an entire 0.13 millisecond (assuming the preferred duty cycle rate of 3.8 kHz) while proceeding to assert the LSBs, (bits 6 through 0, in any sequence, their order of assertion being functionally immaterial) of the even pixels, which collectively comprise an overall duration equal to that of the MSBs. Next the microcontroller asserts the MSB of the even pixels, because the allotted duration for the odd MSB has expired, followed by the LSBs of the odd pixels, and so on, through the entire set of bits. This alternating odd/even approach also more evenly distributes the blinking patterns so that all the LEDs on a given line are not blinking in unison when in the worst-case scenario where the same image data is sent to many adjacent pixels, which is quite common. This further provides masking of any aliasing of dark and light moray patterns that might manifest themselves if the display is filmed or videotaped at a frame rate slightly more or less than that of the display.

In the exemplary embodiment discussed throughout, even pixel bits 7 and odd pixel bits 6 are asserted at the same time, then the odd pixel bits 0 to 5 are asserted upon the end of the odd pixel bits 6s' allotted duration. Next, the odd pixel bits 7 and even pixel bits 6 are asserted at the same time upon the co-incident terminations of the odd pixel bits 7 and the even pixel bits 5s' allotted duration. Then the odd pixel bits 0 to 5 are asserted after which the cycle repeats. This methodology groups the execution of PWM assertion bit fields for situational programming convenience. The odd

pixel bits 7/even pixel bits 6-0, then even pixel bits 7/odd pixel bits 6-0 sequence described above is essentially preserved.

Modified LED Subpixel Color Arrangement

The present invention is also of a method and apparatus **100** for positionally balancing subpixel LEDs useful for portions of displays that are occluded by overhangs. The subpixel LEDs are positionally balanced so that specific colored LEDs are not allocated exclusively to upper/lower or right/left subpixel positions. This positional balance is employed to eliminate any color balance distortions that arise when some LEDs are obscured by light shields or other occluding member. Light shields, which are commonly employed in LED displays, are typically comprised of narrow strips of opaque material which are affixed above a horizontal strip of LEDs and overhang the LEDs slightly to provide shading against sunlight or other unwanted stray or ambient light. Partial occlusion of LEDs by the light shields can occur when the viewer is observing from a position below the display at an angle that is substantially off axis from a line drawn normal to the display. In this case, the light shield that is above any given strip of LEDs then also occludes some of the light emitted from the strip of LEDs in the next row above.

A preferred embodiment of the invention to eliminate or reduce color balance distortions from such occlusions is as follows (see Fig. 6): Two red LEDs **102** are placed with one unit in the upper left and one in the lower right position of the pixel. In each odd numbered pixel, the green LED **106** is placed in the lower left; the blue LED **104** is placed in the upper right. In each even numbered pixel, the green **110** and blue **108** LEDs exchange positions. Consequently, if pixels are partially obscured in a manner that is uniform to all of the pixels in a general area, the net effect is that each color will be obscured proportionately. Thus, the proportion of the intensity of each color with respect to the others remains unchanged, and the color balance will remain unaffected. In the invention, positioning of colored subpixels are not homogenous across the whole display, and the invention may be employed for pixels having any number of subpixels, variations between pixels other than simply odd/even variations, reversed positionings of red versus green/blue LEDs, subpixels light sources other than LEDs, and like variations.

Edge Mounted LED Configuration

The invention is further of a method and apparatus **120** for mounting display panel LEDs on edges of printed circuit boards (PCBs). In the invention, LEDs are mounted edgewise to each PCB, allowing a higher density of LEDs per unit area, and additionally allowing superior heat dispersion and removal. Each of the PCBs, constituting a partial row of the display, preferably carries 64 pixels, although within a given display system any convenient number of pixels per row board can be employed. Adding additional row boards above or below the first one allows the display to be built up stack-like in the vertical dimension as desired. Adding corresponding stacks of row boards adjacent to the first allows the display to be built to the desired horizontal size.

The conventional method of mounting LEDs for a display is to place them all on a single planar surface (or several coplanar surfaces that abut tightly and therefor effectively serve as one). If the planar surface incorporates a PCB, the necessity of providing electrical connections to each LED (or modular cluster of LEDs) limits the allowable density, because connection points and/or driving electronics will additionally require space on the circuit board. A variation in the planar system of mounting is to make wire or cable connections directly to each LED terminal (or modular cluster of LEDs), which may thereby allow a higher density, but this results in intricate and expensive wiring systems. Mounting LEDs to a planar surface also tends to concentrate heat at this plane, making heat removal increasingly difficult at higher LED densities.

In the present invention, referring to Figs. 7-10, the LEDs **124** are mounted along the edge of the PCB **122** with the legs **126** of the LEDs preferably unbent and uncut, and soldered or otherwise affixed to metal pads **128** positioned along the length of one edge of the PCB.

The pads are preferably set on both the top surface and bottom surface of the PCB. The two legs of each LED connect to a corresponding pair of pads on either the top surface or the bottom surface. For each pixel, which consists of four individual LEDs, preferably two mount on the top surface and two mount on the bottom surface of the same PCB. Alternatively, the bottom row of LEDs on a PCB can form the top two subpixels and the top row of LEDs on a PCB below can form the bottom two subpixels. The LEDs on each surface are touching each other, or nearly touching,

and they also contact the LEDs mounted on the opposite surface. By this means, a maximum density can be achieved whereby pixels can be packed together at a repeating interval of distance corresponding to the width of two LEDs, plus a slight allowance for dimensional tolerance. Each PCB, now carrying a row of LEDs, is spaced from the adjacent PCB by this same interval of distance. This spacing is measured center-to-center, i.e., from the center point of the edge of one PCB to the center point of the edge of the adjacent PCB.

The advantages of this mounting of LEDs are several. A very high density can be achieved, but without any significant increase in the difficulty of connecting to the LEDs. The driving circuitry is preferably placed on the same PCB as the LEDs, and connects to the LEDs by ordinary metal circuit board traces. The drive electronics and the connections to the LEDs do not take away any area from the viewing surface of the display because in this new system neither of these is located in the same plane as the viewing surface. In addition, the two legs of each LED are left uncut and are soldered for most of their length to long mounting pads on the PCB (the legs may, but preferably do not, extend past the interior ends of the mounting pads). Because a large portion of the heat that is generated in an LED can be conducted away from the LED through its metal mounting legs, the unwanted heat is drawn to and spread out at the substantial surface area of the long mounting pads and is then further removed from the system by, preferably, forced air cooling. The LED mounting of the present invention, therefore, affords a significant advantage over a planar mounted system in that the invention efficiently conducts heat away from the viewing surface where it is generated.

The invention permits very high density, high brightness LED displays to be emplaced. Displays of greater than approximately 5,000 lumens/m^2 and up to at least approximately 35,000 lumens/m^2 (and up to 50,000 lumens/m^2 for brief periods, such as for flashes) are deployable with the invention.

Lead-Vaned Heat Convection Plenum

Referring to Fig. 11, another method and apparatus **140** for removing excess heat from display LEDs is to use the full, untrimmed length of the LED **142** leads **144** as they come from the factory as convection vanes in a forced-air plenum **146**. Preferably, the normal perpendicular

insertion of the LED leads is made through two printed circuit (PC) boards **148,150** preferably spaced as far apart as the length of the untrimmed leads will allow. That is, the untrimmed LED leads are inserted as far into the first (or front) PC board layer as possible then affixed (preferably by solder or cement) to this front PC board **148** layer. The LED leads then are inserted through the second (or rear) PC board **150** far enough for both leads of each LED to be affixed. Power and ground can be routed to the LEDs through one or both of the PC boards, while space between the PC boards (typically about an inch, but limited only by the length of the LED leads) acts as a forced-air plenum for convection cooling of the LEDs.

This design affords three basic advantages. One, it allows for the removal of excess heat inherent in high-density, high-brightness LED configurations. Two, it facilitates weatherproofing by offering a flat, easily sealed surface against which the LEDs may be abutted. Three, it allows for automated LED handling (tape and reel) and placement (through-hole) during the manufacturing process.

Industrial Applicability:

The invention is further illustrated by the following non-limiting example of the bit-by-bit methodology of the present invention.

Example

Assume that a color intensity value of 165, 10100101 in binary, has been received for application at a given LED and assume a PWM frequency of approximately 3.8 kHz. The microcontroller examines the MSB, the leftmost bit 7, and sends it to the latch that controls that LED and lets that latch remain unchanged for 1/2 of a PWM cycle or 0.13 (0.26/2) milliseconds. In this case the bit = 1 so the latch is asserted and the LED is illuminated for 0.13 milliseconds. The next bit, bit 6 = 0, is sent to the latch which is de-asserted turning the LED off and is then left unaltered for 1/4 of a PWM cycle or 0.065 milliseconds. Next, bit 5 = 1 is sent to the latch and the LED is illuminated for 1/8 of a cycle or 0.0325 milliseconds. Then bit 4 = 0 is de-asserted at the latch for 1/16 or 0.01625 milliseconds.; bit 3 = 0 is de-asserted for 1/32 cycle or 8.125 microseconds; bit 2 = 1 is asserted for 1/64 cycle or 4.062 microseconds; bit 1 = 0 is de-asserted for 1/128 cycle or 2.031

microseconds; and finally bit 0 = 1 is asserted for 1/256 cycle or 1.015 microseconds. The desired ratio of illuminated period to total cycle period or duty cycle is 165 / 256 or 0.64453125. The total time illuminated was bit 7 + bit 5 + bit 2 + bit 0 or 0.13 + 0.0325 +0.004062 + 0.001015 = 0.1696 milliseconds. The total cycle period = 0.2631 milliseconds. The duty cycle = 0.1696 / 0.2631 = 0.64453125.

Although the invention has been described in detail with particular reference to these preferred embodiments, other embodiments can achieve the same results. Variations and modifications of the present invention will be obvious to those skilled in the art and it is intended to cover in the appended claims all such modifications and equivalents. The entire disclosures of all references, applications, patents, and publications cited above are hereby incorporated by reference.

CLAIMS

What is claimed is:

1. A display, said display comprising:

at least one position-independent sub-panel;

a digital video interface for distributing digital image data to and from said at least one position-independent sub-panel; and

a computer for image generation and storage.

2. A method of distributing data to a display, the method comprising the steps of:

a) providing a display comprising at least one position-independent sub-panel;

b) providing a computer for distributing image data to the display;

c) generating images in the computer for distribution to the display;

d) distributing digital image data between the computer and the sub-panel(s) with a digital video interface; and

e) displaying the images on the display.

3. A display control apparatus comprising a plurality of latches for asserting image data to subpixels of a display according to bit position of the data.

4. A color display apparatus comprising a plurality of pixels, each pixel comprising a plurality of subpixels, each subpixel being selected from a group consisting of two or more colors, wherein a color arrangement of said subpixels is not homogenous across all pixels.

5. A color display apparatus comprising a plurality of LEDs mounted to an edge of a printed circuit board and oriented parallel to said printed circuit board.

6. An LED display apparatus comprising a brightness of at least approximately 50,000 lumens/m^2.

7. A display apparatus comprising a plurality of LEDs each comprising leads connected to and passing through a first printed circuit board and affixed to a second circuit board, thereby creating a plenum in a space between said first and said second printed circuit boards.

8. A display control apparatus comprising a plurality of low voltage digital signaling (LVDS) transmitter/receiver pairs for transmitting digital video interface (DVI) data to a plurality of sub-panels of a display.

9. A display subpixel switched current source comprising an NPN transistor, a current sensing resistor connected between an emitter of said NPN transistor and ground, a PNP transistor, a reference voltage applied to a base of said PNP transistor, and a light emitting diode connected to a collector of said NPN transistor, wherein a switching current is applied to an emitter of said PNP transistor.

10. A display comprising:

a plurality of position-independent subpanels each comprising a subpanel control mechanism comprising:

a low voltage digital signaling receiver;

a low voltage digital signaling transmitter; and

a programmable control device; and

a low voltage digital signaling for distributing digital image data to and from said plurality of subpanels;

wherein said programmable control device is programmed to receive subpanel position information through low voltage digital signaling control lines from an adjacent subpanel control mechanism and to pass updated subpanel position information to another adjacent subpanel.

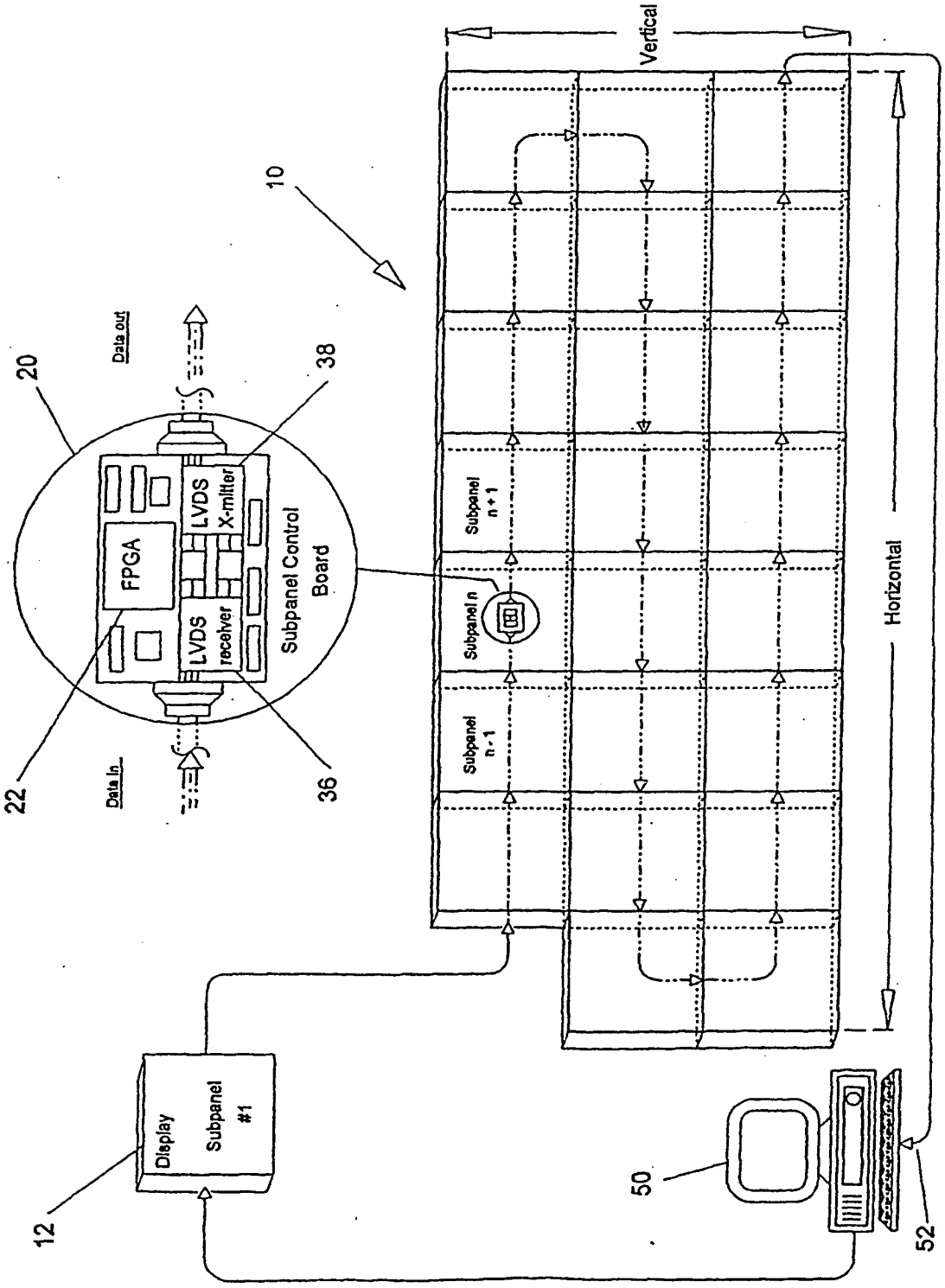


Fig. 1

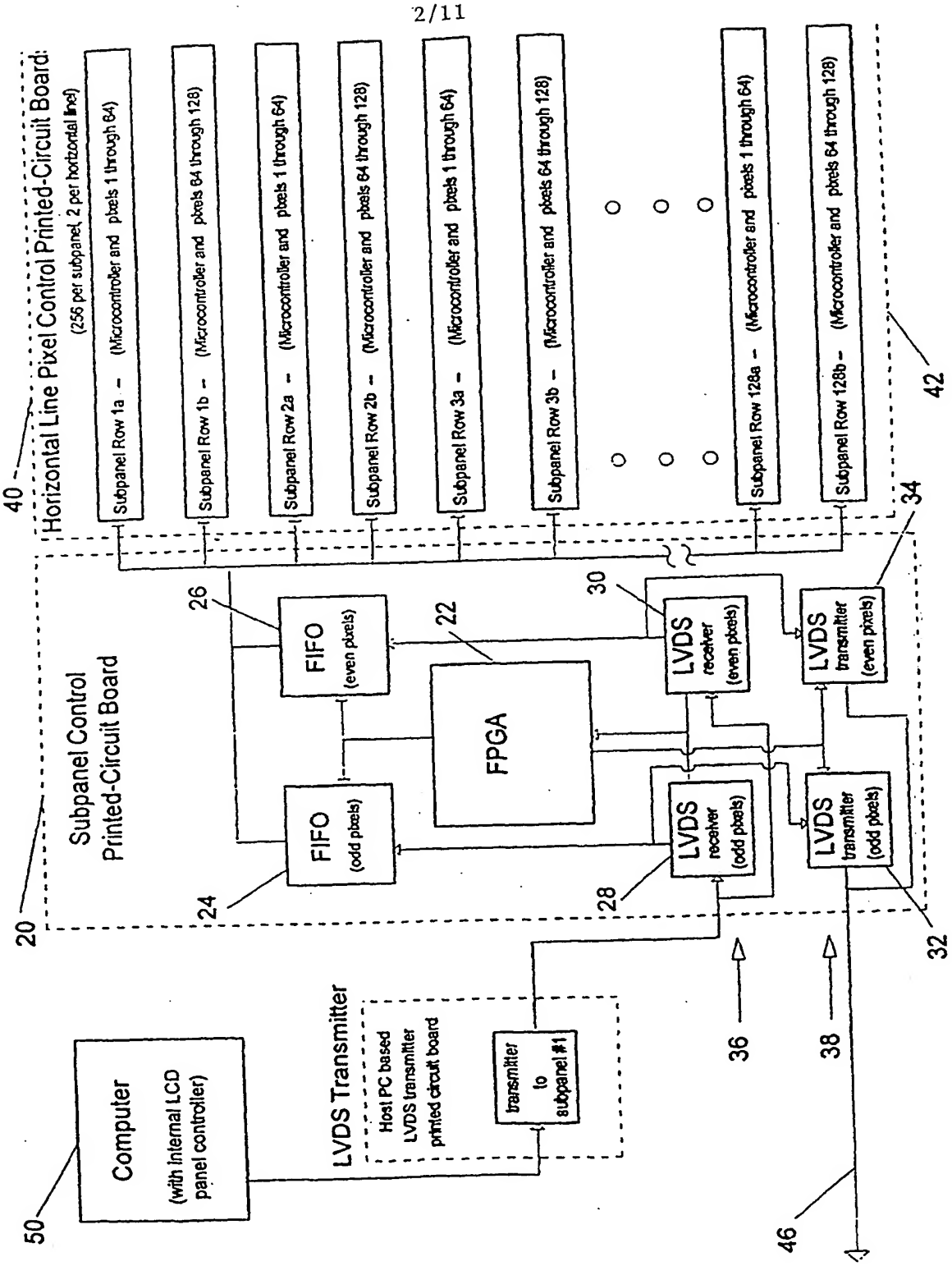


Fig - 2

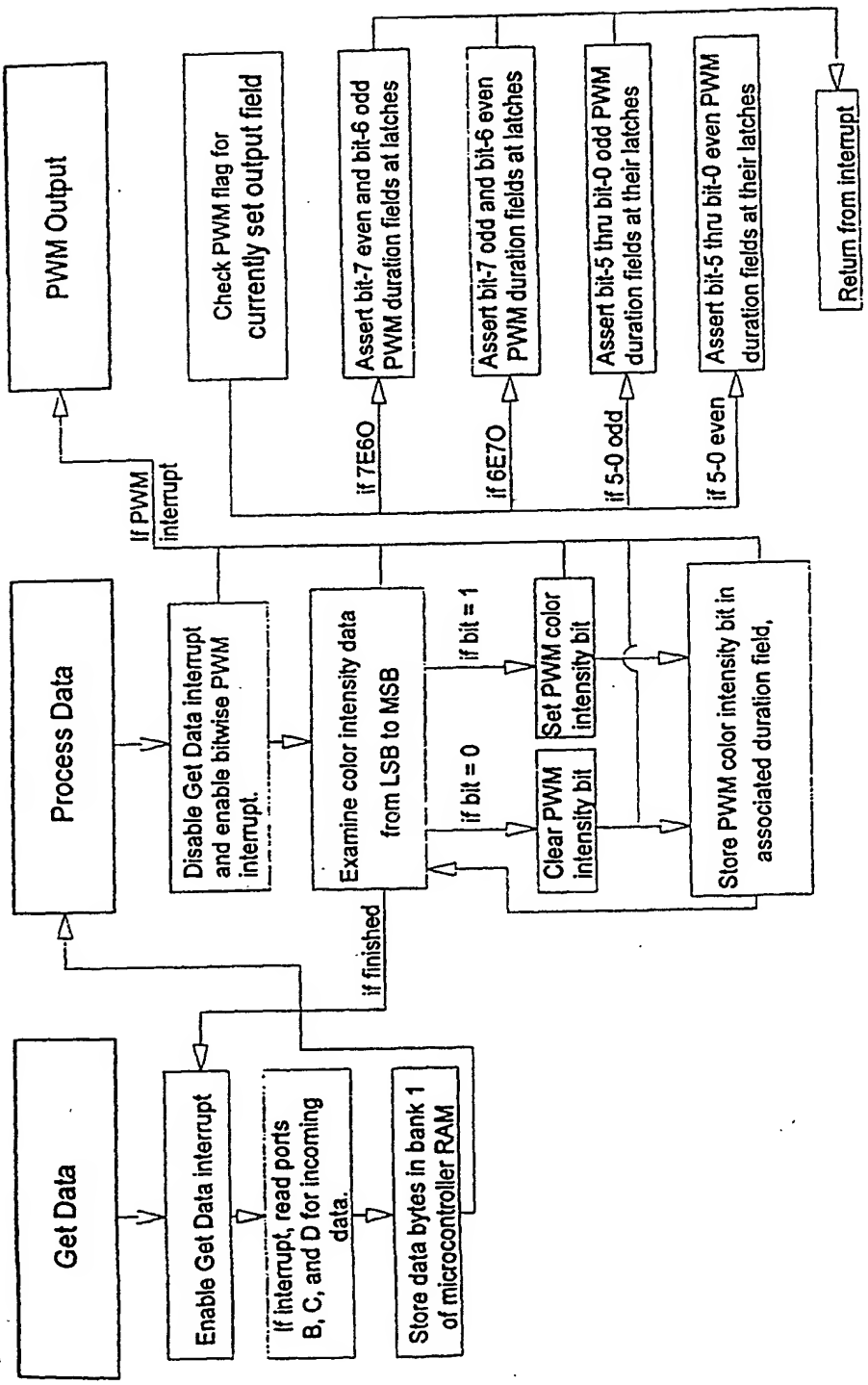


Fig. - 3

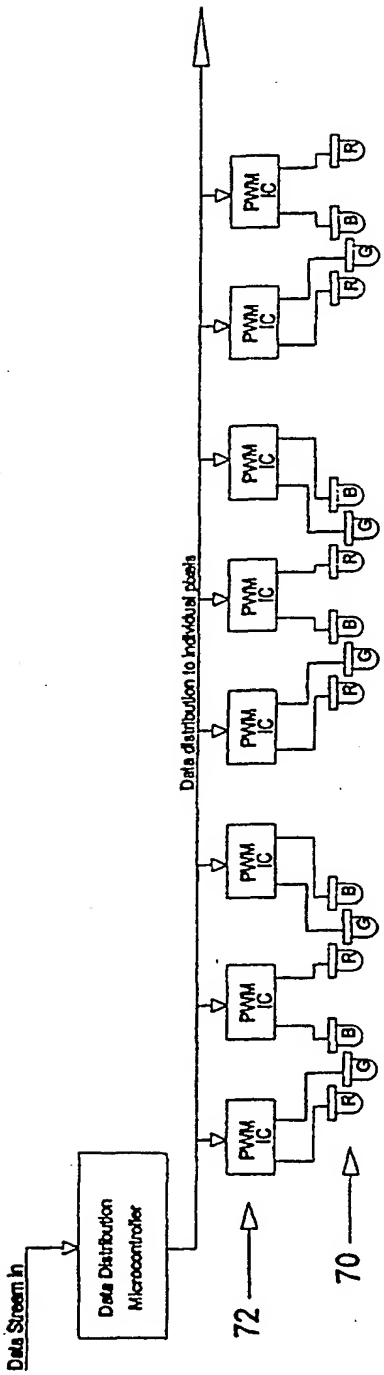


Fig. - 4A Prior Art

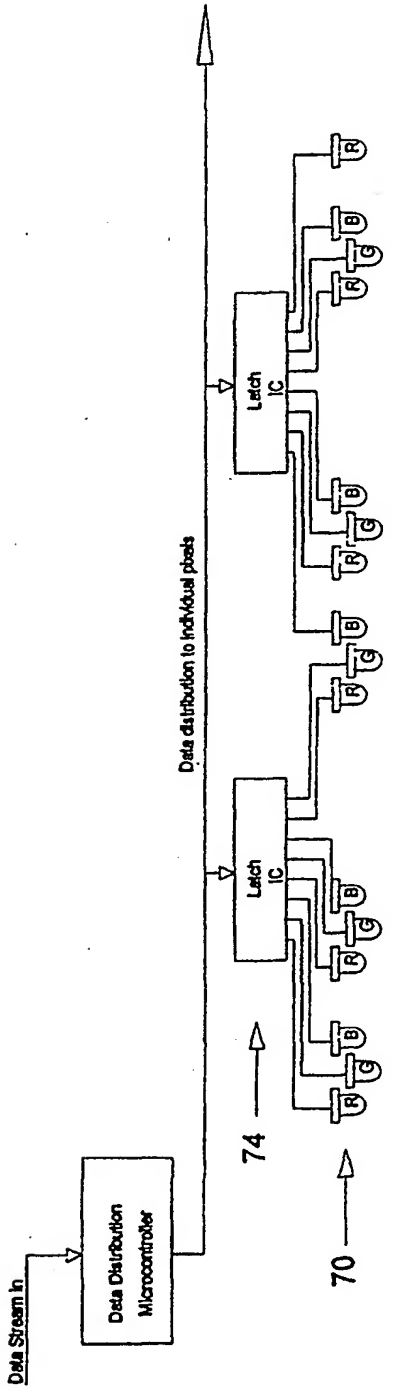


Fig. - 4B PWM using Latch ICs

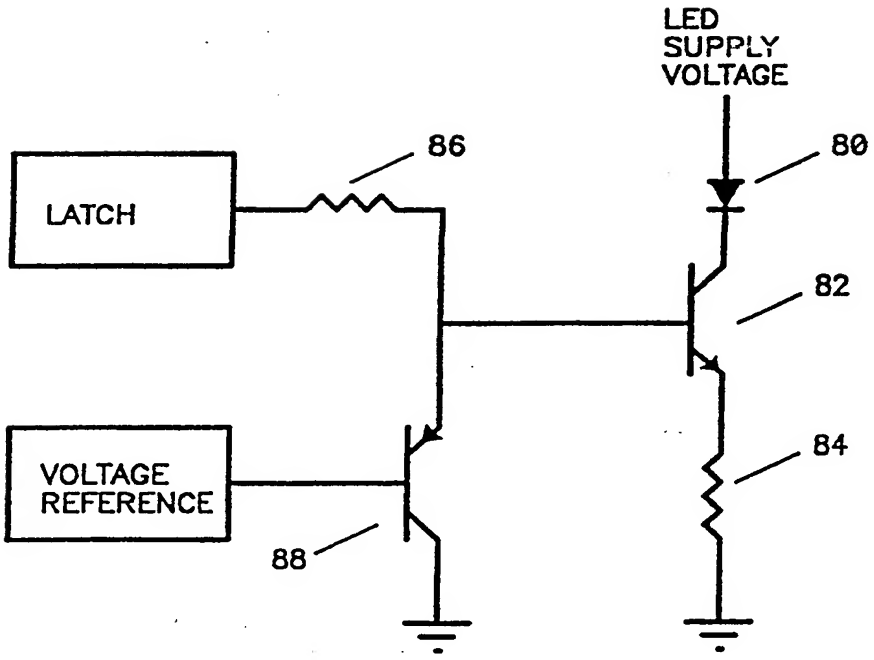


FIG. 5

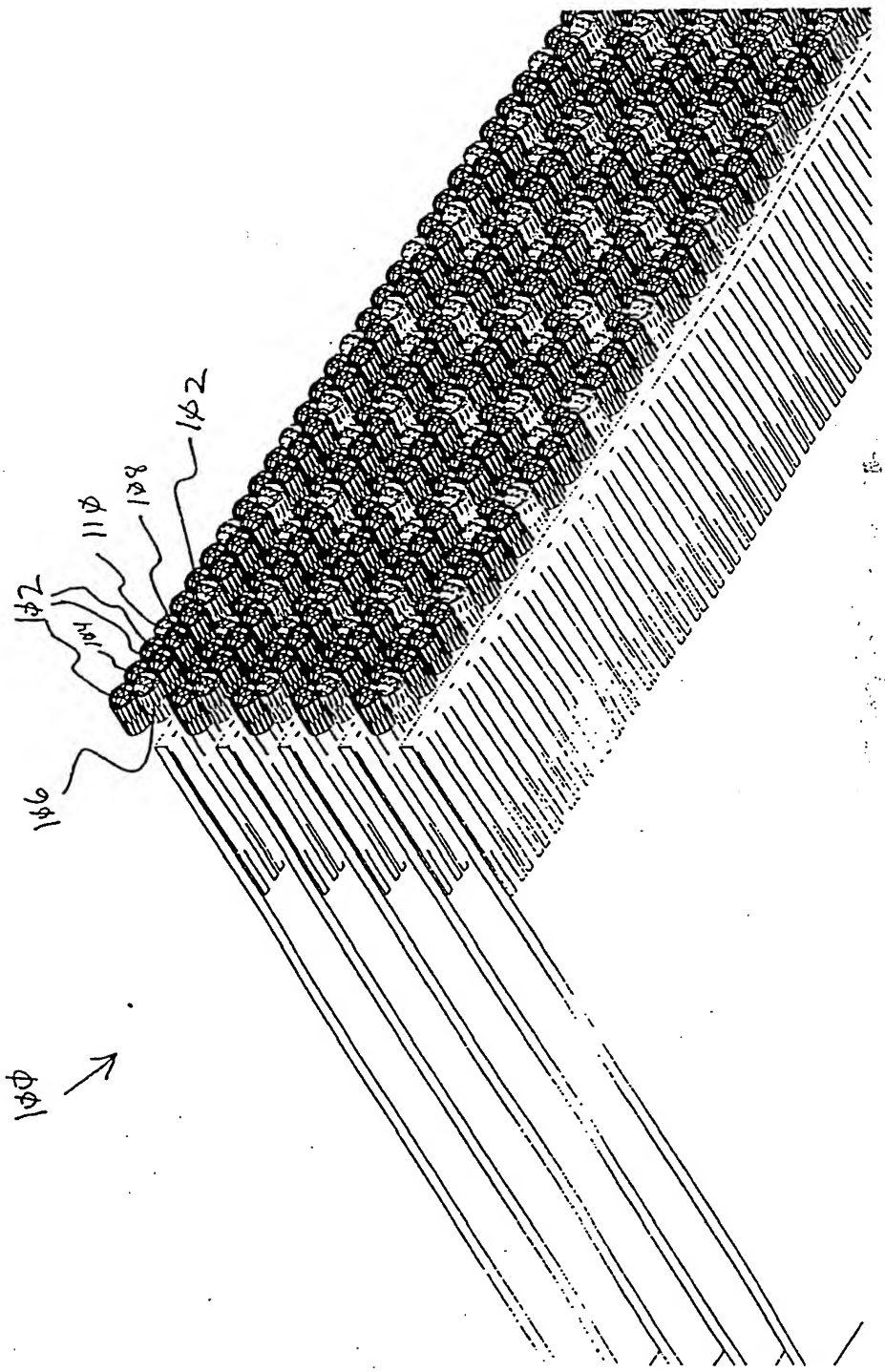


Fig. 6

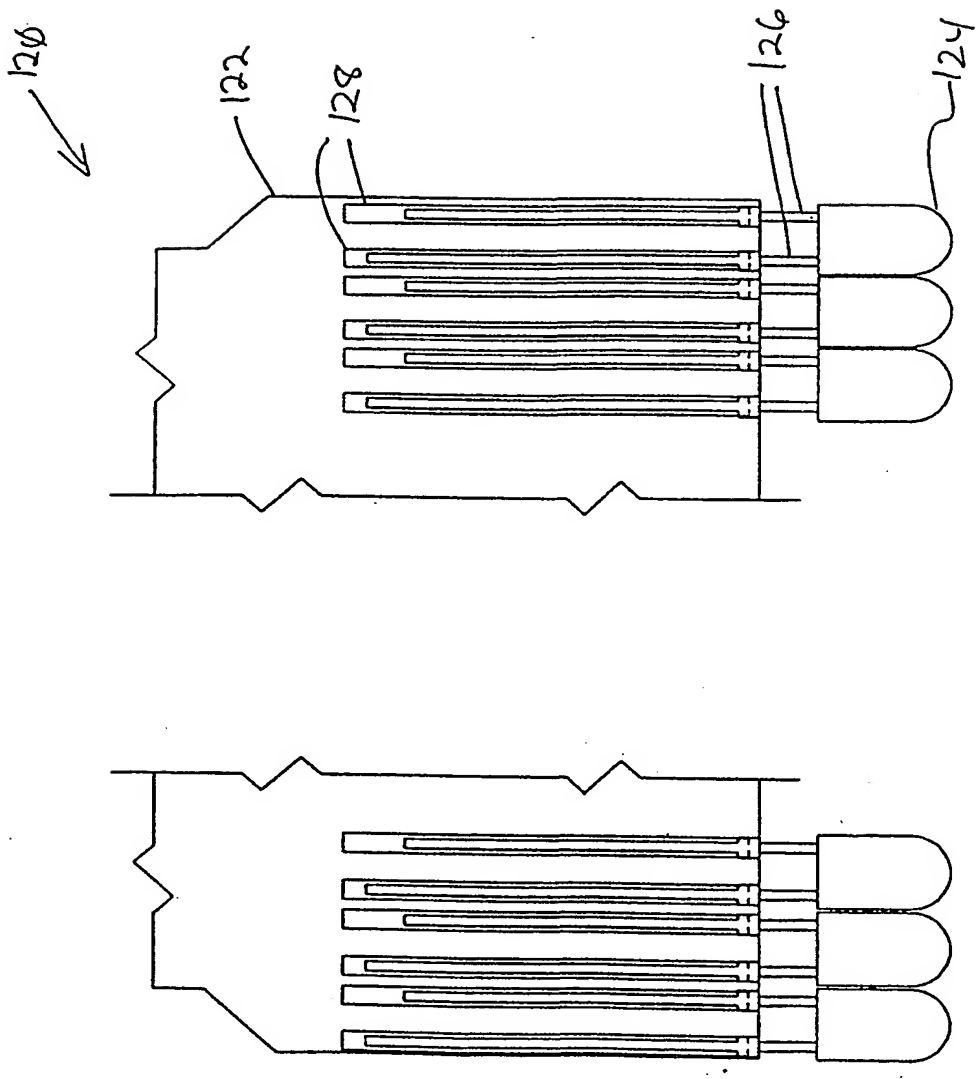


Fig. 7

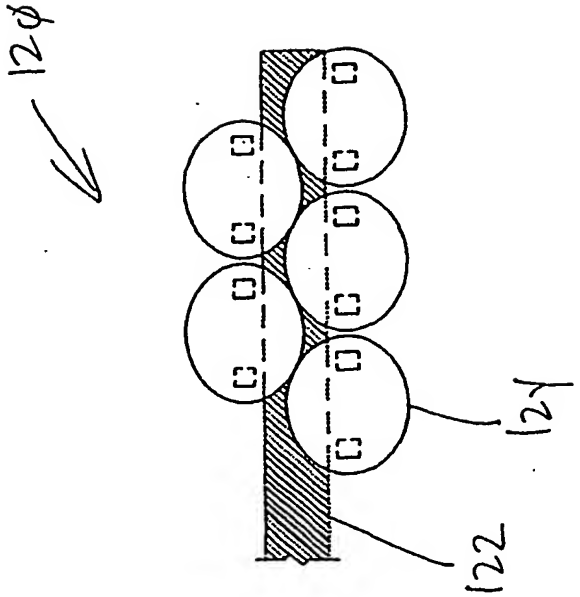
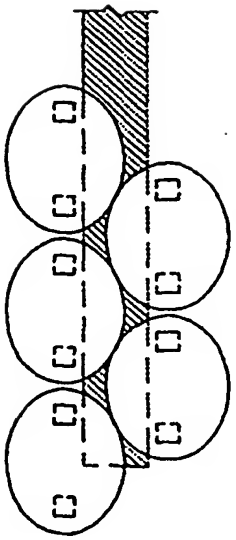


Fig. 8



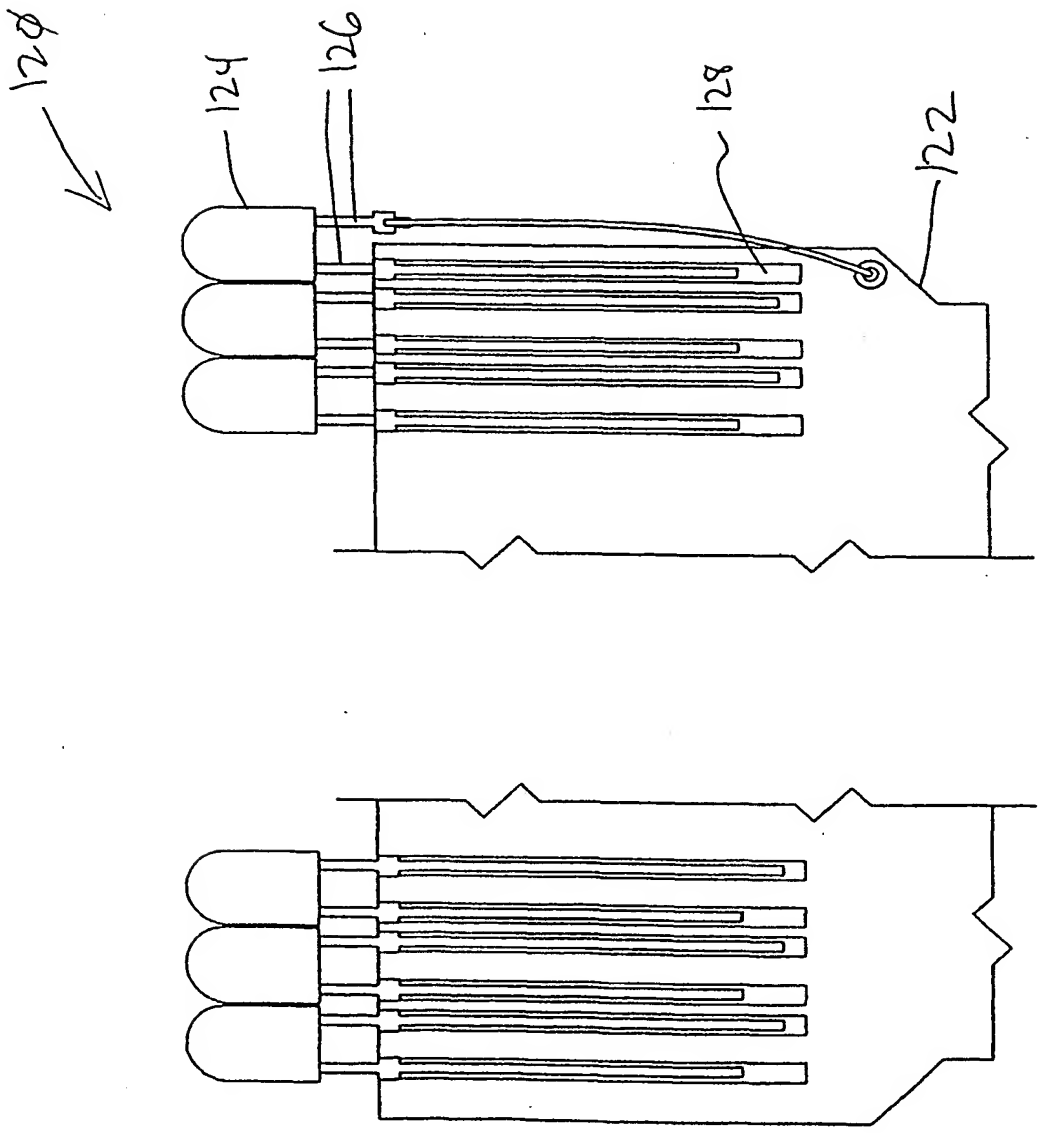


Fig. 9

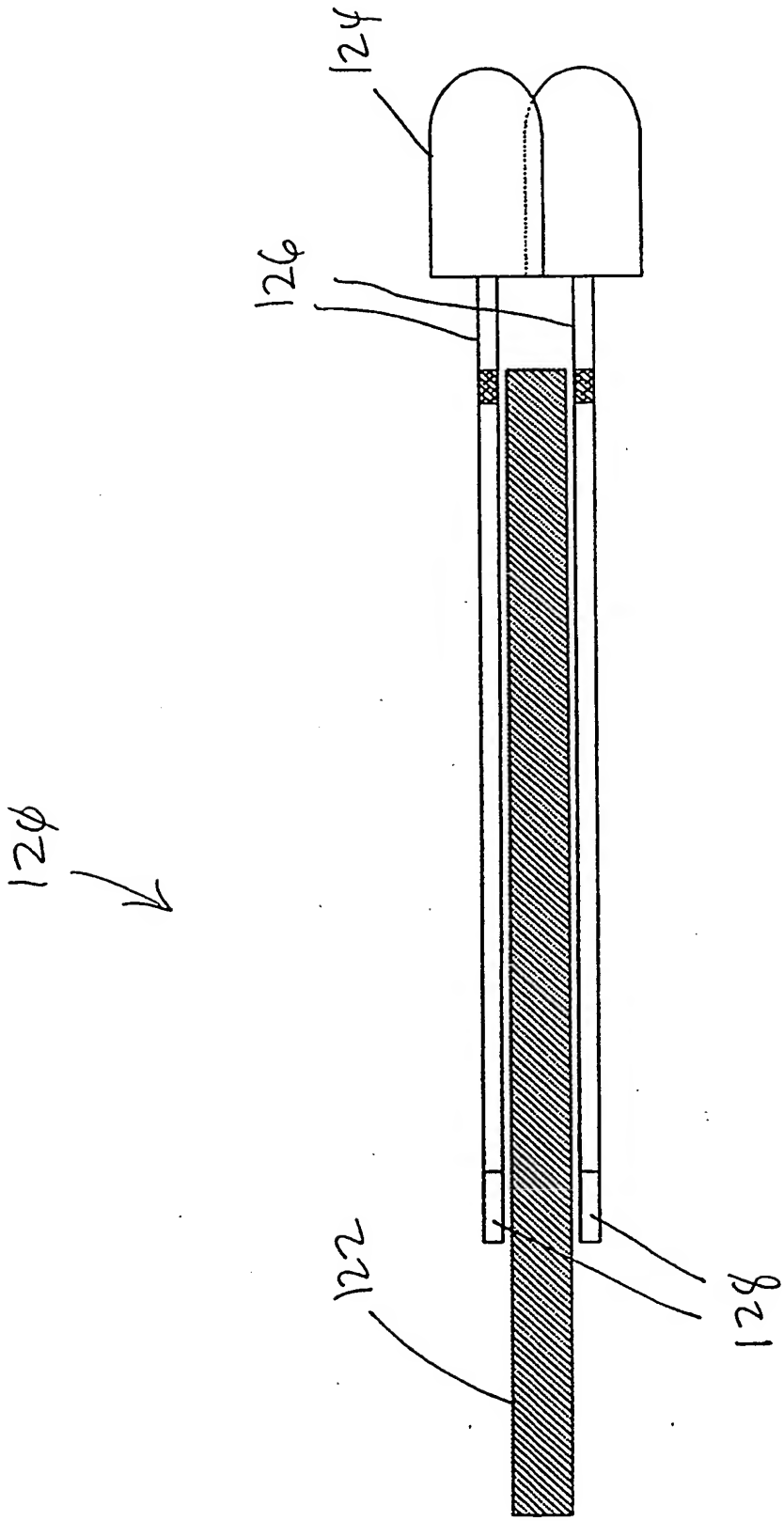


Fig. 10

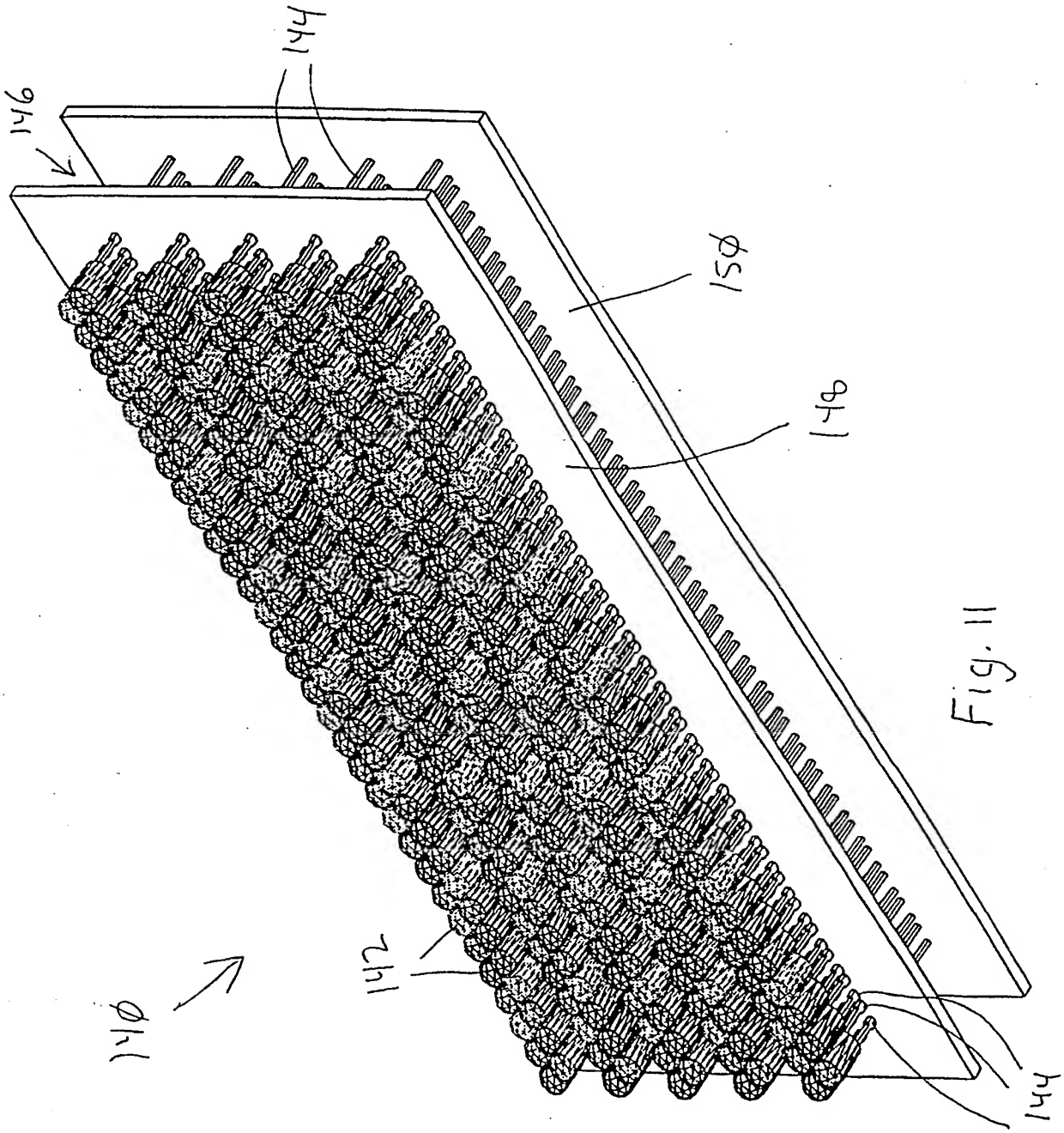


Fig. 11

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US01/17816

A. CLASSIFICATION OF SUBJECT MATTER

IPC(7) :G09G 5/00
US CL :345/3.1, 82

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 345/3.1, 82

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

East 1.01

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 5,736,967 A (KAYSER et al) 07 April 1998, col. 3, lines 42-62, col. 6, lines 20-31, col. 7, lines 30-39, col. 8, lines 1-12, col. 10, lines 29-35, and col. 15, lines 15-34.	1-9
Y,P	US 6,219,011 B1 (ALONI et al) 17 April 2001, col. 7, lines 40-55, col. 12, lines 47-56, and col. 14, lines 42-49.	1-9

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search 30 JUNE 2001	Date of mailing of the international search report 11 OCT 2001
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer RICARDO OSORIO Telephone No. (703) 308-4700

Form PCT/ISA/210 (second sheet) (July 1998)*